Automatic Code Generation for Integrated Circuit Design

ABSTRACT

An integrated circuit is designed by interconnecting pre-designed data-driven cores (intellectual property, functional blocks). Hardware description language (e.g. Verilog or VHDL) and software language (e.g. C or C++) code for interconnecting the cores is automatically generated by software tools from a central circuit specification. The central specification recites pre-designed hardware cores (intellectual property) and the interconnections between the cores. HDL and software language test benches, and timing constraints are also automatically generated from the central specification. The automatic generation of code simplifies the interconnection of pre-existing cores for the design of complex integrated circuits.